What is claimed is:

1. A digital signal processing device comprising:

multiplication means for multiplying an input ΔΣ modulation signal generated from ΔΣ modulation by a factor;

ΔΣ modulation means having a plurality of integrators for varying effective orders and applying ΔΣ modulation again to an output from said multiplication means; and

switchover means for switching between a reprocessed ΔΣ modulation signal from said ΔΣ modulation means and said input ΔΣ modulation signal.

2. The digital signal processing device according to claim 1, wherein said ΔΣ modulation means comprises order control means for varying effective orders depending on signal switchover situations in said switchover means.

3. The digital signal processing device according to claim 2, wherein said order control means varies effective orders for said ΔΣ modulation means at an approximate timing when said switchover means switches between said input ΔΣ modulation signal and said reprocessed ΔΣ modulation signal.

4. The digital signal processing device according to claim 2, wherein said order control means varies effective orders for said ΔΣ modulation means at an approximate timing when said switchover means switches between a fixed signal changing to no sound in an audible band and music data processed with ΔΣ modulation.

5. The digital signal processing device according to claim 1, wherein said ΔΣ modulation means comprises fraction elimination means for eliminating a fraction remaining in said integrator.

6. A digital signal processing method, comprising steps of:

a multiplication step for multiplying an input ΔΣ modulation signal generated from ΔΣ modulation by a specified factor for specified processing;

a reprocessed ΔΣ modulation step for reapplying ΔΣ modulation to an output provided with said specified processing by using a ΔΣ modulator comprising a plurality of integrators for varying effective orders; and

a switchover step for switching between said input ΔΣ modulation signal and said reprocessed ΔΣ modulation signal.

7. The digital signal processing method according to claim 6, wherein said reprocessed ΔΣ modulation step varies effective orders for said ΔΣ modulator depending on signal switchover situations in said switchover step.

8. The digital signal processing method according to claim 7, wherein said reprocessed ΔΣ modulation step varies effective orders for said ΔΣ modulator at an approximate timing when said switchover step switches between said input ΔΣ modulation signal and said reprocessed ΔΣ modulation signal.

9. The digital signal processing method according to claim 7, wherein said reprocessed ΔΣ modulation step varies effective orders for said ΔΣ modulator at an

approximate timing when said switchover step switches between a fixed signal changing to no sound in an audible band and music data processed with ΔΣ modulation.

10. The digital signal processing method according to claim 6, wherein said reprocessed ΔΣ modulation step not only varies effective orders for a ΔΣ modulator, but also eliminates a fraction remaining in said integrator.

11. A ΔΣ modulator for applying ΔΣ modulation to a multi-bit signal comprising:

a plurality of integrators; and

order variation means for varying effective orders increasing due to connection with a plurality of said integrators.

12. The ΔΣ modulator according to claim 11, wherein the fraction elimination means for eliminating a fraction remaining in said integrator.